Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled).

2. (New) A semiconductor memory device comprising:

a memory cell array having a plurality of memory cells arranged in rows and columns, said memory cells storing data and being selected according to address signals; and

a control circuit, receiving a clock signal and a first control signal, configured to output a plurality of said data in synchronism with said clock signal after said first control signal is asserted, output of said data beginning a number of transition (N) of an internal signal (N being a positive integer $\geq$ 2) which responds to said clock signal after said first control signal is asserted, at least one of said data being output at the transition of said internal signal after said output begins.

3. (New) A semiconductor memory device according to claim 2, wherein said control circuit receives said address signals on a transition of said clock signal after said first control signal is asserted.

4. (New) A semiconductor memory device according to claim 2, wherein said control circuit further receives row address signals for selecting said memory cells and a second control signal, said control circuit receiving said row address signals on a transition of said clock signal after said second control signal is asserted.

5. (New) A semiconductor memory device according to claim 2, wherein said first control signal is a pulse signal.

6. (New) A semiconductor memory device comprising:

a memory cell array having a plurality of memory cells arranged in rows and columns, said memory cells being selected on an address signal; and

a control circuit configured to receive a first signal having a first state and a second state, and a second signal having a third state and a fourth state, and configured to output a plurality of data stored in said memory cells responding to said first signal, after a third signal switches N times ($N \geq 2$, N is a positive integer) between a fifth state and a sixth state in response to said first signal switching between the first state and the second state after said second signal switches between said third state and said fourth state.

7. (New) A semiconductor memory device according to claim 6, wherein said control circuit receives said address signal when said first signal switches between said first state and said second state after said second signal switches between said third state and said fourth state.

8. (New) A semiconductor memory device according to claim 6, wherein said control circuit further receives an address signal used to select said memory cells and receives a fourth signal having a seventh state and an eighth state, said control circuit receives said address signal when said first signal switches between said first state and said second state after said fourth signal switches between said seventh state and said eighth state.

9. (New) A semiconductor memory device according to claim 8, wherein said address signal is a row address signal.

10. (New) A semiconductor memory device according to claim 6, wherein said control circuit further receives a column address signal when said second signal switches between said third state and said fourth state.

11. (New) A semiconductor memory device according to claim 6, wherein said control circuit comprises a count circuit configured to count a number of times said third signal switches between said fifth stated and said sixth state.

12. (New) A semiconductor memory device according to claim 6, wherein said second signal is a pulse signal.

13. (New) A semiconductor memory device according to claim 6, wherein a period of said first signal is from about 10 nanoseconds to about 15 nanoseconds.

14. (New) A semiconductor memory device according to claim 6, wherein said control circuit further receives a sixth signal having an eleventh state and a twelfth state, and said control circuit delays the output of said plurality of data based on a number of switches of said third signal counted while said sixth signal is in said twelfth state.

15. (New) A semiconductor memory device according to claim 6, wherein said control circuit further receives a sixth signal having an eleventh state and a twelfth state, and said control circuit negates the third signal counted while said sixth signal is in said twelfth state.

16. (New) A semiconductor memory device according to claim 6, wherein said control circuit further receives a fifth signal having a ninth state and a tenth state and a seventh signal having a thirteenth state and a fourteenth state, and said control circuit receives and fifth signal when the first signal changes between said first state and said second state while said seventh signal is in said fourteenth state.